ABSTRACT OF THE DISCLOSURE

A self-programmable chip for real-time estimation, prediction, and control includes a reconfigurable array processing network for compatibility with Very Large Scale Integration (VLSI). The reconfigurable array processing network provides a feed-forward neural network and learning modules, wherein a synapse cell structure (10) provides synapse cells (100) having on-chip learning integrated therein. The chip has a control cell structure (20) including at least one control cell (110) providing digital memory and control modules supplying ordered signal routing functionality and operational modes for the chip.